UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,256	06/19/2001	Jingsong Xia	31075-7 EQ3	3823

7590 10/17/2005

Troy J. Cole
Woodard, Emhardt, Naughton, Moriarty and McNett
Bank One Center/Tower
111 Monument Circle, Suite 3700
Indianapolis, IN 46204-5137

EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,256	XIA ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 26th, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 19th, 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-13 are pending in the application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 8-9, 11-12 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of copending Application No. 09/876,547 (PG-Pub No. 2002/0191716). Although the conflicting claims are not identical, they are not patentably distinct from each other.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding to Claim 8, the claim merely broadens the scope of the copending application claim 3, by eliminating the" mapper" between the trellis decoded signal and the decision feedback equalizer. The subject matter claimed in the instant application is fully disclosed in the patent and is

covered by the copending application since the copending application and the instant application are claiming common subject matter.

Regarding to Claims 9 & 11, the claims provide further limitation to the parent claims by disclosing the trellis decoder to be a Viterbi decoder. It is obvious to one of ordinary skill in the art at the time of the invention that the trellis decoder can be implemented using the Viterbi algorithm. The selection of the Viterbi Algorithm, to implement the trellis decoder, is a matter of design choice and there is no criticality in implementing this algorithm.

Regarding to Claim 12, the claim provides further limitation to the parent claim by disclosing the Viterbi decoder to have 16 stages. It is obvious to one of ordinary skill in the art at the time of the invention that the Viterbi decoder comprises multiple stages, and the implementation of the Viterbi decoder with 16 stages is a matter of design choice and there is no criticality in implementing the decoder with 16-stages.

4. Claims 10 & 13 are provisionally rejected under the judicially created doctrine of double patenting over copending Application No. 09/876,547 (PG-Pub No. 2002/0191716). This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

Regarding to Claim 10, the subject matter claimed in the instant application is fully disclosed in the referenced copending application, Claim 3, and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: An adaptive equalizer

comprising a trellis decoder, a mapper, and a decision feedback equalizer; wherein the information from the trellis decoder passes through the mapper before it is input into the decision feedback equalizer.

Regarding to Claim 13, the subject matter claimed in the instant application is fully disclosed in the referenced copending application, Claim 5, and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: An adaptive equalizer comprising an FIR filter; a trellis decoder coupled to the FIR filter; a mapper; a decision feedback equalizer coupled to the FIR filter and the trellis decoder via the mapper; wherein the decoded output is mapped and scaled by the mapper and used by the adaptive equalizer to generate an error signal.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

5. Claims 1-6 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over copending Application No. 09/876,547 (PG-Pub No. 2002/0191716) in view of Birru (PG-Pub No. 2002/0172275).

This is a provisional obviousness-type double patenting rejection.

Regarding to Claims 1 & 3-6, the subject matter claimed in the instant application is fully disclosed in the referenced copending application, Claim 3,

and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: An adaptive equalizer comprising a trellis decoder; a mapper coupled to the decoded output; a decision feedback equalizer coupled to the mapped output. The claims also disclose that the decoder is a Viterbi decoder further comprising 16-stages. It is obvious to one of ordinary skill in the art at the time of the invention that the trellis decoder can be implemented using the Viterbi algorithm, and that the Viterbi decoder comprises multiple stages, therefore, the selection of the Viterbi Algorithm, to implement the trellis decoder and further implementing the decoder with 16-stages, is a matter of design choice and there is no criticality in implementation of the decoder algorithm as described above. Furthermore, it is also obvious that a decision feedback equalizer can be implemented as a filter with multiple taps depending on the accuracy and computational complexity desired, and the selection of 16-taps is a matter of design choice and there is no criticality in implementing the DFE as described above.

Birru discloses the implementation of a trellis decoder in combination with a decision feedback equalizer (Fig. 9). Birru further discloses the implementation such that each decoder output stage is mapped to a respective one of the taps of the equalizer (Fig. 8 & Fig. 10) wherein the error signal is generated from the final decoding stage.

Regarding to Claim 2, the subject matter claimed in the instant application is fully disclosed in the referenced copending application, Claim 5, and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: the claim provides a further limitation to the parent claims by disclosing the adaptive equalizer to further comprise a FIR filter. This limitation and the limitations of the parent claims are fully disclosed in the "Claim 5" of the above referenced copending application, and the above discussion in regards to the parent claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birru (PG-Pub No. 2002/0172275) in view of Applicant Admitted Prior Art (AAPA).

Regarding to Claim 1 & 3-12, Birru discloses an adaptive equalizer (Fig. 9) comprising a Viterbi decoder having multiple stages and producing a decoded output (Fig. 9, element 250 & Fig. 15, element 250 & Paragraphs 58-60 & Fig. 10, elements 1030-1060); a decision feedback equalizer (DFE) having

multiple taps (Fig. 9, element 720 & Fig. 15, element 1520 & Fig. 10, element 720); wherein the output of the decoder stages is mapped to the respective taps of the decision feedback equalizer such that the taps receive the output from the earliest decoding stages (Fig. 10 & Fig. 12). However, Birru does not specify the Viterbi decoder having 16 stages and the decision feedback equalizer having more than 16 taps and a mapper element between the decoder and the decision feedback element.

The AAPA discloses a method and apparatus for decoding data in a digital wireless communication system using a Viterbi decoder (Specification, Page 7, lines 11-23 & Fig. 3, element 350 & Fig. 6). The AAPA further discloses a trellis encoder to include a symbol mapper; wherein implementing a Viterbi decoder is implemented to decode the encoded data (Specification, Page 7, lines 5-12 & Fig. 4). The AAPA further discloses the viterbi decoder to include a number of stages, most often 16 or 24 (Specification, Page 7, lines 11-14). The AAPA further discloses the input into the decision feedback equalizer is the output of the mapper (Specification, Page 6, lines 15-16). The AAPA further discloses the decision feedback equalizer to include "M" stages (Specification, Page 6, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Thomas teaches implementing a Viterbi decoder comprising 16 stages and a mapper so as to generate a mapped scaled output and this can be implemented in the adaptive equalizer as described in Birru such that the taps of the decision feed back equalizer receive as input the mapper output from

the respective stages of the viterbi decoder so as to compared the decoded/recoded data to the encoded received data so as to avoid error propagation within the data packet. Furthermore, there is no criticality in implementing the decision feed back equalizer with more than 16 taps or fewer than 16 taps, the selection depends on the accuracy or the complexity (computation time) desired in implementing the adaptive equalizer, therefore the selection of the number of taps is a matter of design choice.

Regarding to Claim 2 & 13, Birru in view of AAPA discloses an adaptive equalizer comprising a viterbi decoder, a mapper coupled to the decoder output, a decision feed back equalizer (DFE) coupled to the output of the mapper, wherein the input to each of the respective taps of the DFE is the output of the respective decoder stages via the mapped output as described above. Birru also discloses the adaptive equalizer further comprising an FIR filter (Fig. 9, element 710 & Fig. 10, element 710 & Fig. 15, element 1510 & Fig. 8 & Paragraphs 72-73). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Birru in view of AAPA satisfies the limitations of the claims.

Response to Arguments

8. Applicant's arguments filed on July 26th, 2005 have been fully considered but they are not persuasive. In regards to the arguments presented the Double Patenting rejections have been maintained.

9. Applicant's arguments, in regards to the Prior Art Rejections, with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

    - If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)-272-3056
    - The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
    - Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600